Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A parallel architecture digital filter receiving p input signals (I_0, ...,I_i,...I_{p-1}) and delivering p output signals (S_0,..., S_i,..., S_{p-1}) which are the sums of the input signals weighted with M coefficients (C_0, C_1,..., C_{M-1}), this filter comprising p parallel channels (V_0,..., V_i,...,V_{p-1}) receiving the input signals (I_0,..., I_i,..., I_{p-1}), characterized in that it comprises r+1 stages (E_0,..., E_j,...,E_r), where r is the integer portion of ratio ~~(m+p-2)/2~~ (M+p-2)/2, the stage of rank j delivering p intermediate signals (R_0^j,...R_i^j,...R_{p-1}^j) which are the weighted sums of the input signals defined by:

$$R_i^j = \sum_{q=0}^{p-1} (C_{M-I-q+i-jp}) I_{q+jp}$$

the filter further comprising a summing means (Σ) receiving said intermediate signals (R_i^j) and delivering p sum defined by:

$$S_i = \sum_{j=1}^{r} R_i^j$$

these p sums forming p output signals [[(]](S_0,...,S_i,...S_{p-1}).

2. (Original) The digital filter according to claim 1, wherein the number of channels p is equal to 2, the filter then comprising a first channel with first means (R^p) for storing the samples of even rank (I_k^p, I_{k-1}^{pi},...) and a second channel with second means (R^i) for storing the samples of odd rank (I_k^i,I_{k-1}^i,...), each channel further comprising first (M_0^p, ..., M_1^p,...ADD^p) and second (M_0^i, ..., M_1^i,...,ADD^i) means respectively, for respectively calculating even (S_k^p) and odd (S_k^i) weighted sums, respectively.

3. (Currently amended) The filter according to claim2, wherein the first and the second means for calculating the even and odd weighted sums each comprise multipliers (M_1^p, M_3^p,..., M_0^i, M_2^i...) each receiving a sample (I_{k-1}^p, I_k^p,..., I_{k-1}^i, I_k^i...) and a weighting coefficient (C_1, C_3, C_0, C_2) (C_0, C_2, C_1,C_3), and an adder (ADD^i, ADD^p) connected to the multipliers.

4. (Currently amended) The filter according to claim2, wherein the first and the second storing means each comprises a first (R^p) and a second (R^i) shift register, respectively.

5. (Currently amended) The filter according to claim 4, wherein each shift register (R^p, R^i) comprises cells (B^p) (B^i) arranged in series, each cell consisting of a flip-flop with a input (D) and a direct output (Q), wherein the input of a flip-flop of rank k is connected to the direct output (Q) of the ~~preceding~~ flip-flop of rank k-1 and the direct output (Q) of ~~a~~ the flip-flop of rank k is connected to the input of the ~~next~~ flip-flop of rank k+1, each flip-flop further comprising a complemented output (!Q), the multipliers then being multiplexers (MPX^p) (MPX^i) with two inputs connected to the direct (Q) and complemented (!Q) outputs of the flip-flops, respectively, each multiplier further comprising a control input receiving a positive or negative control signal (C_0, C_1,..., C_{m-1}) and an output, which is either connected to one of the inputs, or to the other, according to the sign of the control signal.

6. (Original) A receiver for direct sequence spread spectrum signals comprising:

- at least an analog/digital converter (CAN(I), CAN(Q)) receiving a spread spectrum signal and delivering digital samples of this signal,

-at least a digital filter (F(I), F(Q)) with coefficients (C_j) adapted to the spread spectrum sequence, this filter receiving the samples delivered by the digital/analog converter and delivering a filtered signal,

-means (DD, Inf/H, D) for processing the filtered signal able to restore the transmitted data (d), this receiver being characterized in that the digital filter (F(I), F(Q)) is a parallel architecture digital filter according to any of claims 1 to 5.

7. (Currenlty amended) The receiver according to claim 6, comprising first and second channels in parallel, the first (I) for processing a signal in phase with a carrier and the second (Q) for processing a signal in phase quadrature with said carrier, each channel comprising said parallel architecture digital filter (F(I), F(Q)) with, for the first channel (I), notably, first and second adders ($ADD(I)^p$, $ADD(I)^i$) delivering first and second weighted sums ($S(I)_k^p$, $S(I)_k^i$) and, for the second channel (Q), notably, first and second adders ($ADD(Q)^p$, ~~(~~$ADD(Q)^i$) delivering first and second weighted sums ($S(Q)_k^p$, $S(Q)_k^i$).

8. (Currently amended) The receiver according to claim 7, wherein the ~~processing means comprise, in the~~ first channel (I)~~,~~ comprises a first differential demodulation circuit (DD(I)) and ~~in~~ the second channel (Q)~~,~~ comprises a second differential demodulation circuit (DD(Q)), the first differential demodulation circuit (DD(I)) receiving the first weighted sums ($S(I)_k^p$, $S(Q)_k^p$) delivered by filters (F(I), F(Q)) of the first and second channel (I), (Q), and delivering ~~two~~ a first DOT and a first CROSS signals (DOT^p, $CROSS^p$), the second differential demodulation circuit (DD(Q)) receiving the second

weighted sums ($S(I)_k^i$) and ($S(Q)_k^i$) delivered by filters (F(I), F(Q)) of the first and second channels (I, Q) and delivering ~~two~~ a second DOT and a second CROSS signals (DOT^i, $CROSS^i$).

9. (Currently amended) The receiver according to claim 8, ~~wherein the processing means further comprise~~ comprising a clock and an information circuit (Inf/H) receiving the (DOT^p, $CROSS^p$), (DOT^i, $CROSS^i$), signals delivered by the first and second differential demodulation circuits (~~DOT~~DD(I), DD(Q)) and delivering two even and odd information signals (S_{inf}^p), S_{inf}^i), a clock signal (SH) and a parity signal (Sp/i).